IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Lines et al.	Attorney Docket No.: FULCP006
Application No.: 10/667,152	Examiner: LI, AIMEE J.
Filed: September 16, 2003	Group: 2183
Title: ASYNCHRONOUS MULTIPLE-ORDER ISSUE SYSTEM ARCHITECTURE	Confirmation No. 8727

CERTIFICATE OF EFS-WEB TRANSMISSION
I hereby certify that this correspondence is being transmitted electronically through EFS-WEB to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450 on **June 3, 2008.**

Signed: / Emma Durrell /
Emma Durrell

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants request review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reasons stated below.

The Examiner has failed to establish a prima facie case of unpatentability.

The Examiner has ignored important limitations in the claims which are neither shown nor suggested by the art of record. In particular, the combination of the Vegesna and Chu references does not teach or suggest "N parallel pipelines" in which "data units are issued to the respective pipelines staggered in time such that up to N data units enter the N pipelines during the average cycle time." The failure of these references to teach or suggest this limitation is thoroughly articulated in the Applicants' most recent response.

In the Examiner's response to the Applicants' arguments in the Final Office Action mailed May 13, 2008, the Examiner stated that Vegesna, not Chu, teaches this limitation. See section 51 on page 20. However, in the previous office action mailed on October 17, 2007, the Examiner explicitly stated the opposite of this proposition, i.e., that Vegesna does NOT teach this limitation and that Chu does. See sections 8 and 9 on pages 4 and 5. Notwithstanding this

confusing reversal by the Examiner, the Applicants respectfully submit that neither of these contradictory positions is supportable.

As set forth in previous responses, Vegesna describes synchronous parallel pipelines which process parallel data units *simultaneously*, and therefore require elaborate measures to determine whether there are any dependencies between the data units and, if any are found, manipulate the flow of one or both pipelines to handle the dependency. On the other hand, Chu describes the design and operation of a single pipeline, and provides no teachings or suggestions as to how to implement multiple instances of his pipeline in parallel, much less how to issue data units to multiple pipelines. Neither of the references staggers data unit issuance to parallel pipelines over an average cycle time in the manner described and claimed in the present application; the first because the issuance of instructions is explicitly simultaneous, and the second because it is only a single pipeline.

In addition, as set forth in the previous response, the combination of these references is itself unsupportable. That is, by attempting to incorporate the asynchronous pipeline of Chu into the synchronous system of Vegesna, the Examiner has completely ignored the main thrust of the latter. Vegesna makes it clear that the solution being proposed to the problem of issuing multiple instructions per clock cycle requires the simultaneous issuance of instructions to its pipelines. This feature of Vegesna's solution is stressed as critical because it is necessitated by the constraints of the context in which the solution is implemented, i.e., a synchronous domain controlled by a clock signal. It therefore makes absolutely no sense to suggest, as the Examiner has done here, that one of skill in the art would attempt to incorporate an asynchronous pipeline in this context. Not only would this ignore the entire purpose of Vegesna's approach, it would introduce an entirely new set of technical problems for which neither of the references provides any guidance.

In view of the foregoing, the Applicants respectfully request that the current rejections be withdrawn, and that a Notice of Allowance be issued at the earliest possible date.

I am the attorney or agent acting under 37 CFR 1.34

Respectfully submitted,
Weaver Austin Villeneuve & Sampson LLP

/Joseph M. Villeneuve/

Joseph M. Villeneuve
Reg. No. 37,460

P.O. Box 70250
Oakland, CA 94612-0250
510-663-1100